

CLAIMS

What is claimed is:

- 1 1. A self-aligned transistor, comprising:
2 a first silicon portion on an isolation layer, the silicon portion having
3 formed therein a source region and a drain region separated by a channel
4 region, and having a first side and a second side and a top portion;
5 a gate oxide surrounding the channel on said first side, second side
6 and top portion; and
7 a first, a second and a third silicon gate regions surrounding the first
8 silicon portion about the first side, second side and top portion and the
9 channel region.
- 1 2. The transistor of claim 1 wherein said first silicon portion includes an
2 N+ source and drain region and a P-type channel region.
- 1 3. The transistor of claim 2 wherein said first portion is formed of
2 contiguous deposited polysilicon.
- 1 4. The transistor of claim 3 wherein said second portion is formed of
2 contiguous deposited polysilicon.
- 1 5. The transistor of claim 3 wherein said first gate, second gate, and

2 third gate have an N+ dopant concentration matching the source and drain
3 regions.

1 6. The transistor of claim 3 wherein said first gate region has an N+
2 doping and the second gate region has a P+ doping.

1 7. The transistor of claim 1 wherein said isolation layer comprises a
2 buried oxide region of a silicon-on-insulator substrate.

1 8. The transistor of claim 7 wherein said first silicon portion, first gate,
2 and second gate are formed in a contiguous horizontal plane in said silicon-
3 on-insulator substrate.

1 9. The transistor of claim 1 wherein said first silicon portion has a width
2 in a range between 20 nanometers and 150 nanometers.

1 10. The transistor of claim 1 wherein a gate oxide separates said first
2 and second silicon portions.

1 11. The transistor of claim 1 wherein said gate oxide has a thickness of
2 between 1.2-1.7 nanometers.

1 12. The transistor of claim 1 wherein the first and second polysilicon
2 regions are surrounded by a conformal oxide.

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2 13. A method for manufacturing a dual gate transistor device,
3 comprising:

4 (a) providing a substrate having a buried oxide region;
5 (b) depositing a first nitride mask layer having a pattern overlying
6 a silicon region;

7 (c) forming a trench in said substrate with a depth to said buried
8 oxide;

9 (d) depositing a conformal oxide in said trench;

10 (e) forming vias in said conformal oxide adjacent to said silicon
11 region and removing a portion of said first nitride mask to expose a portion
12 of said silicon region;

13 (f) depositing polysilicon in said vias and on said portion of said
14 silicon region; and

15 (g) implanting an impurity into exposed portions of polysilicon in
16 said trench and of said silicon-on-insulator substrate underlying said second
nitride layer.

1 14. The method of claim 13 wherein said step (c) is performed by:
2 depositing a nitride mask layer; forming a trench window in said nitride

3 mask layer; and etching said substrate to expose said buried oxide.

1 15. The method of claim 13 wherein said step (d) is performed by:
2 depositing a TEOS layer to fill the trench to a level equivalent to said first
3 nitride mask layer.

1 16. The method of claim 13 wherein said step (e) comprises: depositing
2 a gate layer; and
3 etching the vias and the first nitride layer through an opening formed
4 in said gate layer.

5 17. The method of claim 13 wherein said step (f) comprises implanting
6 arsenic at an energy of 15-20 KeV with a zero degree tilt to provide a
7 concentration of $2-4 \times 10^{15}/\text{cm}^2$.

1 18. The method of claim 13 wherein said step (f) comprises depositing
2 phosphorous at an energy of 7-10 KeV with a zero degree tilt to provide a
3 concentration of the impurity in a range of $2-4 \times 10^{15}/\text{cm}^2$.

1 19. The method of claim 13 wherein said step (f) comprises depositing
2 boron at an energy of 1.5-2.5 KeV with a zero degree tilt to provide a
3 concentration of the impurity in a range of $2-3 \times 10^{15}/\text{cm}^2$.

1 20. The method of claim 13 further including the step, between steps (f)
2 and (g), of:
3 polishing the polysilicon and substrate.

1 21. The method of claim 13 further including the step, between said
2 steps (e) and (f), of:
3 growing a gate oxide about the silicon region in said vias.